L Number	Hits	Search Text	DBs	Time Stamp
1	111	((crystallizing or crystallization) with (pzt or ferroelectric)) and (Ti with ((lower or bottom) adj electrode)	USPAT; US-PGPUB	2003/05/02 10:15
2	4	(((crystallizing or crystallization) with (pzt or ferroelectric)) and (Ti with ((lower or bottom) adj electrode)) and (Ti with (migration or migrating)	USPAT; US-PGPUB	2003/05/02 10:12
3	1	((crystallizing or crystallization) with (pzt or ferroelectric)) and (Ti with ((lower or bottom) adj electrode))	EPO; JPO; DERWENT; IBM_TDB	2003/05/02 10:16

US-PAT-NO: 6495412

DOCUMENT-IDENTIFIER: US 6495412 B1

TITLE: Semiconductor device having a ferroelectric capacitor and a fabrication process thereof

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A semiconductor device having a ferroelectric capacitor is formed by the steps of forming a lower electrode on a substrate, applying a rapid thermal annealing process to the lower electrode, depositing, after the step of rapid thermal annealing process, a ferroelectric film on the lower electrode, **crystallizing the ferroelectric** film by applying a thermal annealing process to the ferroelectric film, and forming an upper electrode on the ferroelectric insulation film.

Further, there is provided an adhesion layer 17 having a **Ti**/TiN structure on the interlayer insulation film 15 so as to cover the exposed part of the plug 16, and a lower electrode 18 of Pt is formed on the foregoing adhesion layer 17. The lower electrode 18 is covered by a ferroelectric capacitor insulation film 19 of PZT or PLZT, and an upper electrode of Pt is formed on the ferroelectric capacitor insulation film 19.

Unfortunately, the foregoing approach to convert the lower electrode 18 once into amorphous phase and then to cause a **crystallization** by an RTA process is ineffective for achieving a satisfactory degree of **crystallization** in the lower electrode 18, and no desirable crystal orientation is

obtained in the
ferroelectric capacitor insulation film 19. Further, when a high-temperature
thermal annealing process is applied to the lower electrode 18 in a furnace,
there is a tendency that the hillock phenomenon is induced in the lower
electrode 18, wherein such a hillock caused in the lower electrode 18 decreases
the yield of the semiconductor device.

In the formation of the ferroelectric capacitor as noted above, it is very
important to crystallize the ferroelectric capacitor insulation film 19 by
conducting a **crystallization** process. Further, it is also very important to
control the process of forming the upper electrode 20. Without such a
crystallization process, no desirable property is obtained for the
ferroelectric capacitor.

Conventionally, such a ferroelectric capacitor is formed first by forming
the adhesion layer 17 of the **Ti**/TiN structure and then the lower electrode 18
of Pt by a sputtering process conducted on the interlayer insulation film 15 in
a reducing or inert atmosphere. Next, the ferroelectric capacitor insulation
film 19 of PZT is formed on the lower electrode 18 by a sputtering process. By
forming the lower electrode 18 in a reducing atmosphere or inert atmosphere,
the problem of oxidation of the lower electrode 18 and associated problem of
increase of the resistance are successfully avoided.

Next, the ferroelectric capacitor insulation film 19 is subjected to a
thermal annealing process in an oxidizing atmosphere at a temperature of
typically 700-800.degree. C., and the ferroelectric capacitor insulation film
19 thus formed undergoes a **crystallization**. Thereby, it has been practiced to

conduct the **crystallization** process in an oxidizing atmosphere so that the formation of oxygen defects in the ferroelectric capacitor insulation film 19, caused as a result of diffusion of oxygen atoms from the ferroelectric capacitor insulation film 19 to the lower electrode 18, is successfully compensated for. As a result of the **crystallization, the ferroelectric** capacitor insulation film 19 shows a preferable hysteresis as represented in FIG. 2, with a spontaneous polarization 2Pr.

crystallizing said ferroelectric film by applying a thermal annealing process to said ferroelectric film; and

crystallizing said ferroelectric film by applying a thermal annealing process to said ferroelectric film; and

According to the present invention, **Ti** migrates from an adhesion layer formed underneath said lower electrode to the surface thereof in the form of TiO.sub.x as a result of the rapid thermal annealing process applied to the lower electrode. Thereby, TiO.sub.x thus migrated functions as nuclei of crystal growth and the ferroelectric crystals of the ferroelectric film, which may either of PZT, PLZT, BST or SBT, deposited on the lower electrode grows generally in the <111> direction. Because of the <111> orientation of the ferroelectric film, the spontaneous polarization is of the ferroelectric film is maximized. By conducting the thermal annealing process of the lower electrode only for a short time in the form of RTA, the oxidation of the lower electrode is avoided successfully. Further, the formation of unwanted hillock is avoided successfully.

FIG. 10 is a diagram showing a temperature control

program used for
crystallizing the ferroelectric capacitor of the third embodiment;

Referring to FIG. 3A, a SiO.sub.2 film 32 is formed on a Si substrate 31 by a thermal oxidation process with a thickness of 200 nm, for example, and a lower electrode 33 of Pt is formed on the SiO.sub.2 film 32 by a D.C. sputtering process conducted at a room temperature, with an adhesion layer 33A of **Ti** interposed between the SiO.sub.2 film 32 and the lower electrode 33.

More specifically, the Ti adhesion layer 33A is formed in an Ar atmosphere under the pressure of 10 mTorr with a thickness of about 20 nm as represented in TABLE I below. Further, the lower electrode 33 is formed under the same condition with a thickness of about 100 nm. The deposition of the **Ti** film 33A and the lower electrode 33 is conducted by setting the D.C. plasma power to 1 kW, wherein the deposition of the **Ti** film 33A is conducted for the duration of 10 seconds while the deposition of the lower electrode 33 is conducted for the duration of 20 seconds.

In the present embodiment, it is believed that the thermal annealing process applied to the lower electrode 33 induces a **migration of Ti** atoms from the underlying adhesion layer 33A to the top surface of the lower electrode 33 and the **Ti** atoms thus migrated form TiO.sub.x on the top surface of the lower electrode 33, wherein TiO.sub.x thus formed acts as the nuclei for the growth of the PLZT crystal grains in the <111> direction. About the <111> growth of PLZT crystals from the TiO.sub.x nuclei, reference should be made to Muralt, P., et al., J. Appl. Phys. vol.63, No.7, pp.3835-3841.

In the step of FIG. 6D, it should be noted that the conductive film 63 thus deposited is further subjected to a rapid thermal annealing process in an Ar atmosphere at the temperature of about 650.degree. C. for 1-60 seconds. As a result of the RTA process thus applied to the conductive film 63, the **Ti** atoms cause a **migration** from the underlying **Ti** adhesion layer to the top surface of the conductor film 63, and there are formed TiO.sub.x nuclei on the top surface of the conductive film 63.

More in detail, it is believed that such a depression in the lower electrode 33 is formed as a result of concentration stress to the grain boundary in the lower electrode 33. When the RTA process is applied to the lower electrode 33, the **Ti** atoms cause a **migration** from the underlying adhesion layer to the top surface of the electrode 33 to form the TiO.sub.x compound as explained before, wherein the **migration of the Ti** atoms occurs predominantly along such grain boundaries and there occurs a segregation of the **Ti** atoms to the grain boundary in the lower electrode 33. Due to the growth of the PLZT crystals starting from such grain boundaries of the lower electrode 33, the lower electrode 33 experiences a concentration of stress in such grain boundaries.

Referring to FIG. 9A, a SiO.sub.2 film 132 is formed on a Si substrate 131 with a thickness of about 200 nm by a thermal oxidation process, and a lower electrode 133 is formed on the SiO.sub.2 film 132 by stacking a **Ti** film and a Pt film consecutively under a condition of TABLE VII.

FIG. 11 shows the fatigue of the ferroelectric capacitor 130 thus obtained in comparison with the fatigue of a conventional

ferroelectric capacitor,
wherein the conventional ferroelectric capacitor
represented in FIG. 11 is
formed by **crystallizing** the PLZT film 134 in an oxidizing
atmosphere and by
forming the upper electrode 135 by a sputtering conducted
in an Ar atmosphere.

Referring to FIG. 20, the high-dielectric capacitor 180
is formed on a Si
substrate 181 covered by an adhesion layer 182 of **Ti** and a
diffusion barrier
layer 183 of TiN, and includes a lower electrode 184 of Ru,
a BST film 185
formed on the lower electrode 184, and an upper electrode
186 of Pt formed on
the BST film 185.

The high-dielectric capacitor of the present invention
has a construction
similar to the high-dielectric capacitor of FIG. 20 except
that the **Ti** adhesion
layer 182 and the TiN diffusion barrier layer 183 are
replaced by a single Ta
film and that a Pt electrode is used in place of the Ru
lower electrode 184 and
is fabricated according to the process of FIG. 28 which is
similar to the
process of FIG. 21. Thus, in the description hereinafter,
those parts of the
high-dielectric capacitor corresponding to the parts
described previously are
designated by the same reference numerals and the
description thereof will be
omitted.

More specifically, the fabrication process starts with
the step 21 of FIG.
33 corresponding to the step 1 of FIG. 21 in which the **Ti**
adhesion layer 182,
the TiN diffusion barrier layer 183 and the lower electrode
184 of Ru are
deposited consecutively on the Si substrate 181 by a D.C.
sputtering process
under a substrate temperature of 300.degree. C.,
respectively with the
thicknesses of 20 nm, 50 nm and 500 nm. Further, in the

step 33 corresponding
to the step 2 of FIG. 21, the BST film 185 is formed on the lower electrode 184
of Ru with a thickness of about 30 nm by conducting an R.F. sputtering process
at a substrate temperature of 400.degree. C.

In the case the foregoing crystallization process of the step 23 and the
oxidizing step 24 of FIG. 33 are conducted in the form of a single annealing
step in an oxidizing atmosphere at the temperature exceeding 400.degree. C.,
on the other hand, it was observed that there occurs a substantial oxidation
not only in the lower electrode 184 of Ru but also in the TiN layer 183 or the
Ti layer 182 caused by the oxygen atoms diffused from the BST film 185.
Associated therewith, there tends to occur a formation of irregular surface in
these layers, and the TiN layer 183 may no longer function as the diffusion
barrier. Further, there may be caused a short-circuit between the upper
electrode 186 and the lower electrode 184. It should be noted that the
oxidation of the TiN barrier layer 183 may cause the problem of poor conduction
between the lower electrode 184 and the memory cell transistor.

In the present embodiment, the foregoing various problems are successfully
avoided by conducting the crystallization process and the oxidizing process
separately, and by choosing the temperature of the oxidizing process so that
there occurs no substantial oxidation in the Ru lower electrode 184, TiN
barrier layer 183 or the **Ti** layer 182.

Referring to FIG. 39, the fabrication process starts with the step 31 in
which the **Ti** adhesion layer 182, the TiN diffusion barrier layer 183 and the
lower electrode 184 of Ru are deposited consecutively on

the Si substrate 181
by a D.C. sputtering process conducted at the substrate temperature of
300.degree. C. with respective thicknesses of 20 nm, 50 nm and 500 nm.
Further, in the step 32, the BST film 185 is formed on the Ru lower electrode
184 with a thickness of about 30 nm by a R.F. sputtering process conducted at
the substrate temperature of 400.degree. C.

Referring to FIG. 43, the fabrication process starts with the step 41 in
which the **Ti** adhesion layer 182, the TiN diffusion barrier layer 183 and the
lower electrode 184 of Ru are deposited consecutively on the Si substrate 181
by a sputtering process conducted at the substrate temperature of 300.degree.
C. with respective thicknesses of 20 nm, 50 nm and 500 nm.

Referring to FIG. 44, the fabrication process starts with the step 51 in
which the lower electrode 33 of the Pt/**Ti** structure is formed on the SiO.sub.2
film 32 covering the Si substrate 31 under the condition of TABLE VI. Further,
the PLZT film 34 is formed on the lower electrode 33 in the step 52 under the
condition represented in TABLE 8.

Referring to FIGS. 46A and 46B, it can be seen that the lower electrode 33
of FIG. 46A contains a substantial amount of oxygen and **Ti, while in the lower
electrode** 33 of FIG. 46B, the amount of oxygen 1 and **Ti** is reduced
substantially. The result of FIGS. 46A and 46B suggests that there occurred a
substantial densification in the lower electrode 33 as a result of the first
phase thermal annealing of FIG. 45 which is conducted in the inert atmosphere.

In the present embodiment, it should be noted that the ferroelectric film
134 is not limited to PLZT but the ferroelectric film 134

may be formed of any
ferroelectric or high-dielectric material having the
perovskite structure.
Further, the lower electrode is by no means limited to the
Pt film deposited on
the **Ti** film but may be formed of a refractory metal such as
Ru or Ir, or a
conductive oxide such as RuO.sub.2 or IrO.sub.2.